10-18-00

LIMBACH & LIMBACH L.L.P.
2001 Ferry Building, San Francisco, CA 94111
415/433-4150

Address to:
Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

Attorney's Docket No. NSC1-H1500 [P04809]

First Named Inventor VLADISLAV VASHCHENKO

UTILITY PATENT APPLICATION TRANSMITTAL
(under 37 CFR 1.53(b))

SIR:

Transmitted herewith for filing is the patent application entitled:
BIPOLAR TRANSISTOR-BASED ELECTROSTATIC DISCHARGE (ESD) PROTECTION STRUCTURE WITH A HEAT SINK

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date October 17, 2000, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EM370371647US addressed to: Box Patent Application, Commissioner for Patents, Washington, D.C. 20231.

ELIZABETH A. REICKER — Elizabeth A. Reicker
(Name of person mailing paper) (Signature)

Enclosed are:

1. X Transmittal Form (two copies required)

2. The papers required for filing date under CFR § 1.53(b):
   i. 12 Pages of specification (including claims and abstract);
   ii. 4 Sheets of drawings.
   __ formal X informal

3. Declaration or oath

   a. X Newly executed (original or copy)

4. __ Microfiche Computer Program (Appendix, see 37 CFR 1.96)

5. __ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   i. __ Computer Readable Copy
   ii. __ Paper Copy (identical to computer copy)
   iii. __ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

6. X An assignment of the invention to National Semiconductor Corporation, 2900 Semiconductor Drive, M/S D3-579, Santa Clara, CA 95051-8090 is attached (including Form PTO-1595).

   i. X 37 CFR 3.73(b) Statement (when there is an assignee)

7. __ Power of Attorney

8. X An Information Disclosure Statement (IDS) is enclosed, including a PTO-1449 and copies of 4 references.

9. __ Preliminary Amendment.

10. X Return Receipt Postcard (MPEP 503 -- should be specifically itemized)

11. __ Other

12. FOREIGN PRIORITY

[] Priority of application no. _ filed on _ in _ is claimed under 35 USC 119.

The certified copy of the priority application:

- _ is filed herewith; or
- _ has been filed in prior application no. _ filed on _, or
- _ will be provided.

__ English Translation Document (if applicable)

13. **FEE CALCULATION**

a. __ Amendment changing number of claims or deleting multiple dependencies is enclosed.

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee ($710)
Total Claims	8 - 20	* 0	x $18.00	0
Independent Claims	1 - 3	* 0	x $80.00	0
__ Multiple dependent claim(s), if any			$270.00	0

*If less than zero, enter "0".

Filing Fee Calculation $710

50% Filing Fee Reduction (if applicable) . . . . . $

14. Small Entity Status

a. __ A small entity statement is enclosed.
b. __ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
c. __ is no longer claimed.

15. Other Fees

X Recording Assignment [$40.00] $40

__ Other fees
Specify _____ . . . . . $

Total Fees Enclosed $750

16. Payment of Fees

X Check(s) in the amount of $ 750 enclosed.

__ Charge Account No. 12-1420 in the amount of $__.

A duplicate of this transmittal is attached.

17. All correspondence regarding this application should be forwarded to the undersigned attorney:

Mayumi Maeda
Limbach & Limbach L.L.P.
2001 Ferry Building
San Francisco, CA 94111
Telephone: 415/433-4150
Facsimile: 415/433-8716

18. Authorization to Charge Additional Fees

X The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 12-1420. **A duplicate of this transmittal is attached.**

LIMBACH & LIMBACH L.L.P.

October 16, 2000
(Date)

By: _____
Mayumi Maeda, Reg. No. 40,075
Attorney(s) or Agent(s) of Record

Attorney Docket No. NSC1-H1500 (P04802)

PATENT

BIPOLAR TRANSISTOR-BASED ELECTROSTATIC DISCHARGE (ESD) PROTECTION STRUCTURE WITH A HEAT SINK

INVENTORS: Vladislav Vashchenko and Peter J. Hopper

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor device structures and, in particular, to electrostatic discharge protection structures for use with integrated circuits.

2. Description of the Related Art

Electrostatic Discharge (ESD) protection devices are commonly employed in an integrated circuit (IC) to protect electronic devices in the IC from spurious pulses of excessive voltage (e.g., an ESD event, Human Body Model [HBM] event, or Electrical Overstress [EOS] event). See, for example, S.M. Sze, *Electrostatic Discharge Damage,* in VLSI Technology, Second Edition, 648-650 (McGraw Hill, 1988). A variety of conventional ESD protection devices that make extensive use of diodes, metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar transistors are known in the field.

Conventional bipolar transistor-based ESD protection devices include, for example, bipolar transistor-based transient and bipolar transistor-based static ESD protection devices (e.g., grounded base bipolar transistor-based ESD protection devices and Zener Triggered bipolar transistor-based ESD protection devices). Descriptions of these and other conventional ESD protection structures are available in G. Croft and J. Bernier, *ESD Protection Techniques for High Frequency Integrated Circuits*, Microelectronics Reliability 38, 1681-1689 (1998); *Design and Layout of a High ESD Performance NPN Structure for Submicron BiCMOS/Bipolar Circuits*, J.Z. Chen et al., *Design and Layout of a High ESD Performance NPN Structure for Submicron BiCMOS/Bipolar*

Circuits, 34th Annual IEEE International Reliability Physics Symposium Proceedings, 227-232 (1996); J.C. Bernier et al., *A Process Independent ESD Design Methodology*, IEEE International Symposium on Circuits and Systems Proceedings 1, 218-221 (1999); W.D. Mack et al., *New ESD Protection Schemes for BiCMOS Processes with Application to Cellular Radio Designs*, IEEE International Symposium on Circuits and Systems 6, 2699-2702 (1992), each of which is hereby fully incorporated by reference.

FIG. 1 is a cross-sectional view of a conventional bipolar transistor-based ESD protection structure 10. Conventional bipolar transistor-based ESD protection structure 10 includes a P-type substrate 12, an N-type collector region 14, a P-type base region 16 (e.g., a P-type Si-Ge base region) and an N-type polysilicon emitter 18. The conventional bipolar transistor-based ESD protection structure 10 also includes electrical isolation regions 20 and 22. A metal base contact 24 makes contact with the P-type base region 16 via polysilicon line 26. A metal emitter contact 28 is in contact with the N-type polysilicon emitter 18, while a metal collector contact 30 is in contact with the N-type collector region 14. The metal base contact 24, the metal emitter contact 28 and the metal collector contact 30 each extends through dielectric layer 32.

Electrical schematics illustrating this conventional bipolar transistor-based ESD protection structure 10 arranged in a grounded base bipolar transistor-based ESD protection device and a Zener Triggered bipolar transistor-based ESD protection device are provided in FIGs. 2A and 2B, respectively.

A significant physical limitation of conventional bipolar transistor-based ESD protection structures is their susceptibility to thermal overheating and associated irreversible damage (e.g., local melting). As a consequence, conventional bipolar transistor-based ESD protection structures are unstable in the event that a critical temperature of approximately 1300 °K is reached during an ESD event. Still needed in the field, therefore, is an ESD protection structure for use with bipolar or BiCMOS ICs that is relatively immune to thermal overheating and, thus, stable during an ESD event.

SUMMARY OF THE INVENTION

The present invention provides an ESD protection structure for use with bipolar or BiCMOS ICs that is relatively immune to thermal overheating and, thus, stable during an ESD event. Immunity to thermal overheating during an ESD event is attained in the present invention by employing a heat sink region to dissipate the heat that is generated during such an ESD event.

Bipolar transistor-based ESD protection structures according to the present invention include a semiconductor substrate (e.g., silicon substrate) and a bipolar transistor in and on the semiconductor. The bipolar transistor includes a base region, a collection region and a polysilicon emitter. The bipolar transistor-based ESD protection structures also include a heat sink region disposed above the semiconductor substrate adjacent to the polysilicon emitter (e.g., within a distance of less than 2 microns, preferably less than 1.5 micron). This location is near the point of maximum generated temperature during a transitory ESD event (e.g., a 10 nano-second rising and 150 nano-second falling MIL standard HBM event). By implementing a heat sink region adjacent to the polysilicon emitter, the extra heat capacity of the heat sink region enables heat dissipation during an ESD event. A heat sink region essentially acts as a temporal local heat sink during a short ESD event, thereby increasing ESD protection capability and reliability.

The heat sink region is formed of a material with a heat capacity and/or thermal conductivity that is greater than the heat capacity and/or thermal conductivity of the dielectric layer material (typically an SiO_2-based material) which conventionally covers the ESD protection structures. Therefore, the heat sink region can be formed, for example, of metal (e.g., aluminum, and aluminum alloy, or copper) and/or polysilicon.

In one embodiment of the bipolar transistor-based ESD protection structures according to the present invention, the heat sink region is a floating heat sink region and is disposed above the semiconductor substrate adjacent to the polysilicon emitter within a distance of less than 2 microns, preferably less than 1.5 microns. The electrically floating nature of the floating heat sink

region insures that the electrical behavior (e.g., I-V characteristics and transients) of the remainder of the bipolar transistor-based ESD protection structure is essentially unaltered by its presence.

In another embodiment of the bipolar transistor-based ESD protection structures according to the present invention, a heat sink region is integrated with a metal emitter contact to the polysilicon emitter, thereby making the metal emitter contact "bulky". Such a bulky metal emitter contact acts as a temporal heat sink during a short (e.g., 150 nano-second) ESD pulse.

Bipolar transistor-based ESD protection structures according to the present invention can be thought of as a variant of a bipolar transistor-based ESD protection structure with the distinctive addition of either a floating heat sink region above the semiconductor substrate or a heat sink region integrated with a metal contact (i.e., "bulky" metal contact) to the polysilicon emitter. In either scenario, the heat sink region is disposed adjacent to the polysilicon emitter within a distance of less than 2 microns from the point of maximum generated temperature during a transitory ESD event. Due to extra heat capacity near the point of maximum generated temperature and temporal heat dissipation in such a heat sink region during a short ESD event, bipolar transistor-based ESD protection structures according to the present invention provide immunity to overheating and, consequently, superior ESD protection performance.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description that sets forth illustrative embodiments, in which the principles of the invention are utilized, and the accompanying drawings (in which like numerals are used to designate like elements), of which:

FIG. 1 is a cross-sectional view of a conventional bipolar transistor-based ESD protection structure.

FIGs. 2A and 2B are electrical schematics illustrating a conventional grounded base NPN bipolar transistor-based ESD protection device and Zener Triggered NPN bipolar transistor-based ESD protection device, respectively.

FIG. 3 is a cross-sectional view of a bipolar transistor-based ESD protection structure according to the present invention with a heat sink region.

FIG. 4 is a cross-sectional view of another bipolar transistor-based ESD protection device according to the present invention with a floating heat sink region.

FIG. 5 is a cross-sectional view of a heat sink for use in a bipolar transistor-based ESD protection structure according to the present invention.

FIG. 6 is a graph of temperature versus time from a numerical simulation that illustrates the thermal behavior, during a 2 kV HBM pulse, of various Si-Ge 50 micron bipolar transistor-based ESD protection structures: a bipolar transistor-based ESD protection structure without a metal contact (curve A), a conventional bipolar transistor-based ESD protection structure with a regular metal emitter contact to a polysilicon emitter (curve B) and a bipolar transistor-based ESD protection structure according to the present invention with a heat sink region that is integrated with a metal emitter contact to a polysilicon emitter (curve C).

DETAILED DESCRIPTION OF THE INVENTION

To be consistent throughout the present specification and for clear understanding of the present invention, the following definitions are provided for terms used therein:

The terms "dopant" and "dopants" refer to donor and acceptor impurity atoms (e.g., boron [B], phosphorous [P], arsenic [As] and indium [In]), which are intentionally introduced into a semiconductor substrate (e.g., a silicon wafer) in order to change the substrate's charge-carrier concentration. See, R.S. Muller and T.I. Kamins, *Device Electronics for Integrated Circuits 2nd Edition,* 11-14 (John Wiley and Sons, 1986) for a further description of dopants.

The term "floating," when used in reference to a heat sink, refers to the absence of a direct electrical connection (i.e., a contact) to the heat sink.

FIG. 3 illustrates one embodiment of a bipolar transistor-based ESD protection structure 100 for use with bipolar or BiCMOS ICs according to the present invention. The bipolar transistor-based ESD protection structure 100 includes a P-type semiconductor substrate 112, a bipolar transistor disposed in and on the semiconductor substrate and electrical isolation regions 120 and 122 disposed in and on the semiconductor substrate electrically separating one bipolar transistor from another. The dopant level in the semiconductor substrate can be any conventional level known in the art. The bipolar transistor includes an N-type collector region 114, a P-type base region 116 (e.g., a P-type Si-Ge base region) and an N-type polysilicon emitter 118. A metal base contact 124 makes contact with the P-type base region 116 via polysilicon line 126, while a metal collector contact 130 is in contact with the N-type collector region 114. The bipolar transistor-based ESD protection structure 100 also includes a heat sink region 129 integrated with a conventional metal emitter contact to the N-type polysilicon emitter 118, thereby making the otherwise conventional metal emitter contact bulkier (i.e., possessing an increased heat capacity).

In bipolar transistor-based ESD protection structures for use with 5-7 GHz BiCMOS technology, a considerable improvement of protection capability has been realized by the implementation of a bulky metal emitter contact. When disposed adjacent to the polysilicon emitter within a distance of less than 2 microns from the point of maximum generated temperature during a transitory (e.g., 150 nano-second) ESD event, such a bulky metal emitter contact acts as a temporal local heat sink during the ESD event. Due to its extra heat capacity, heat is dissipated in the bulky metal emitter contact (i.e., heat sink region), thereby increasing the ESD protection capability by 30-50%. The increased ESD protection capability enables more reliable protection for relatively higher HBM pulse amplitude or the use of a smaller bipolar transistor-based ESD protection structure.

FIG. 4 illustrates another embodiment of a bipolar transistor-based ESD protection structure 200 for use with bipolar or BiCMOS ICs according to the

present invention. The bipolar transistor-based ESD protection structure 200 includes a P-type semiconductor substrate 212, a bipolar transistor disposed in and on the semiconductor substrate and electrical isolation regions 220 and 222 disposed in and on the semiconductor substrate electrically separating one bipolar transistor from another. The bipolar transistor includes an N-type collector region 214, a P-type base region 216 (e.g., a P-type Si-Ge base region) and an N-type polysilicon emitter 218. A metal base contact 224 makes contact with the P-type base region 216 via polysilicon line 226, while a metal collector contact 230 and a metal emitter contact 228 are in contact with the N-type collector region 214 and the N-type polysilicon emitter, respectively. The bipolar transistor-based ESD protection structure 200 also includes a floating heat sink region 229 above the semiconductor substrate 212 adjacent to the N-type polysilicon emitter within a distance of less than 2 microns, preferably less than 1.5 microns. This location accumulates heat during an ESD event. A floating heat sink region disposed adjacent to a polysilicon emitter, where heat is known to accumulate during an ESD event, provides temporal local heat capacity and dissipates heat during the ESD event. By providing such extra heat capacity to the otherwise conventional bipolar transistor-based ESD protections structure, ESD protection capability and reliability are significantly increased.

The heat sink regions of FIGs. 3 and 4 have an essentially rectangular cross-sectional shape. Other heat sink shapes can, however, provide the required heat dissipation capability, regardless of whether the heat sink is floating or integrated with a metal emitter contact. A heat sink can, for example, be formed of a plurality of interconnected metal layers and a bulky polysilicon emitter contact. FIG. 5 illustrates a heat sink region 300 manufactured as interconnected 0.35 micron thick metal layers 302, 0.25 micron wide via-like structures 304, 0.35 micron wide contact-like structures 306 and bulky polysilicon emitter contact 308. The heat sink region 300 is surrounded by a conventional dielectric material layer 310. This arrangement provides for a heat sink to be easily manufactured using conventional polysilicon and metal layer deposition and via formation techniques.

Increased ESD protection capability and reliability of bipolar transistor-based ESD protection structures according to the present invention are apparent from FIG. 6. FIG. 6 comparatively illustrates the thermal behavior, during a 2 kV HBM pulse, of various Si-Ge 50 micron bipolar transistor-based ESD protection structures: a bipolar transistor-based ESD protection structure without a metal emitter contact (curve A), with a conventional metal emitter contact (curve B) and with a "bulky" metal emitter contact (curve C).

FIG. 6 suggests that a bipolar transistor-based ESD protection device without a metal contact would attain a maximum generated temperature of approximately 1000 °K, while a bipolar transistor-based ESD protection device with a conventional metal emitter contact would reach a maximum generated temperature of 830 °K. However, a bipolar transistor-based ESD protection device with a bulky metal emitter contact according to the present invention (i.e., with a heat sink) would attain a maximum generated temperature of only 710 °K.

The maximum temperature generated in the bipolar transistor-based ESD protection structure according to the present invention is approximately 15% lower than in the bipolar transistor-based ESD protection structure with a conventional metal emitter contact. A corresponding or greater improvement in ESD protection capability for bipolar transistor-based ESD protection structures according to the present invention is expected. Bipolar transistor-based ESD protection structures according to the present invention can, therefore, provide reliable ESD protection for ESD events of higher amplitude than conventional structures or provide equivalent ESD protection with a smaller structure.

Bipolar transistor-based ESD protection structures according to the present invention can be configured in any known configuration, including grounded base and Zener triggered configurations.

One skilled in the art will recognize that the ESD protection capability and reliability of the bipolar transistor-based ESD protection devices is provided in an analogous manner to that described in U.S. patent application for "MOSFET-Based Electrostatic Discharge (ESD) Protection Structure With a Floating Heat Sink" by the same inventors (filed October 6, 2000; application

number not yet assigned), which is hereby fully incorporated by reference, with respect to MOSFET-based ESD protection devices.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention and that structures within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. A bipolar transistor-based ESD protection structure comprising:

a semiconductor substrate;

a bipolar transistor disposed in and on the semiconductor substrate, the bipolar transistor having a base region, a collection region and a polysilicon emitter; and

a heat sink region disposed above the semiconductor substrate adjacent to the polysilicon emitter.

2. The bipolar transistor-based ESD protection structure of claim 1, wherein the heat sink region is formed of polysilicon.

3. The bipolar transistor-based ESD protection structure of claim 1, wherein the heat sink region is formed of a metal selected from the group consisting of copper, aluminum, alloys of aluminum, titanium and combinations thereof.

4. The bipolar transistor-based ESD protection structure of claim 1, wherein the heat sink region is a floating heat sink region.

5. The bipolar transistor-based ESD protection structure of claim 4, wherein the heat sink region is disposed within 2 microns of the polysilicon emitter.

6. The bipolar transistor-based ESD protection structure of claim 1 further including:

a metal emitter contact to the polysilicon emitter, and wherein the heat sink region is integrated with the metal emitter contact.

7. The bipolar transistor-based ESD protection structure of claim 1, wherein the bipolar transistor is in a grounded base configuration.

8. The bipolar transistor-based ESD protection structure of claim 1, wherein the bipolar transistor is in a Zener triggered configuration.

ABSTRACT OF THE DISCLOSURE

An ESD protection structure for use with bipolar or BiCMOS ICs that is relatively immune to thermal overheating and, thus, stable during an ESD event. This immunity is achieved by employing a heat sink region adjacent to a polysilicon emitter within a distance of less than 2 microns. Such a heat sink region provides temporal heat capacity to locally dissipate the heat generated during an ESD event. Bipolar transistor-based ESD protection structures according to the present invention include a semiconductor substrate and a bipolar transistor in and on the semiconductor. The bipolar transistor includes a base region, a collection region and a polysilicon emitter. The bipolar transistor-based ESD protection structures also include a heat sink region disposed above the semiconductor substrate adjacent to the polysilicon emitter. The heat sink region is formed of a material with a heat capacity and/or thermal conductivity that is greater than the heat capacity and/or thermal conductivity of the material (typically an SiO_2-based material) which conventionally covers the ESD protection structures. The heat sink region can be formed, for example, of metal and/or polysilicon. In one embodiment, the heat sink region is floating and disposed adjacent to the polysilicon. In another embodiment, the heat sink region is integrated with a metal contact to the polysilicon emitter, thereby making the otherwise conventional metal contact bulkier. By locally providing extra heat capacity (i.e., a floating heat sink region or a bulky metal contact), heat is dissipated during an ESD event, thereby increasing ESD protection capability and reliability.

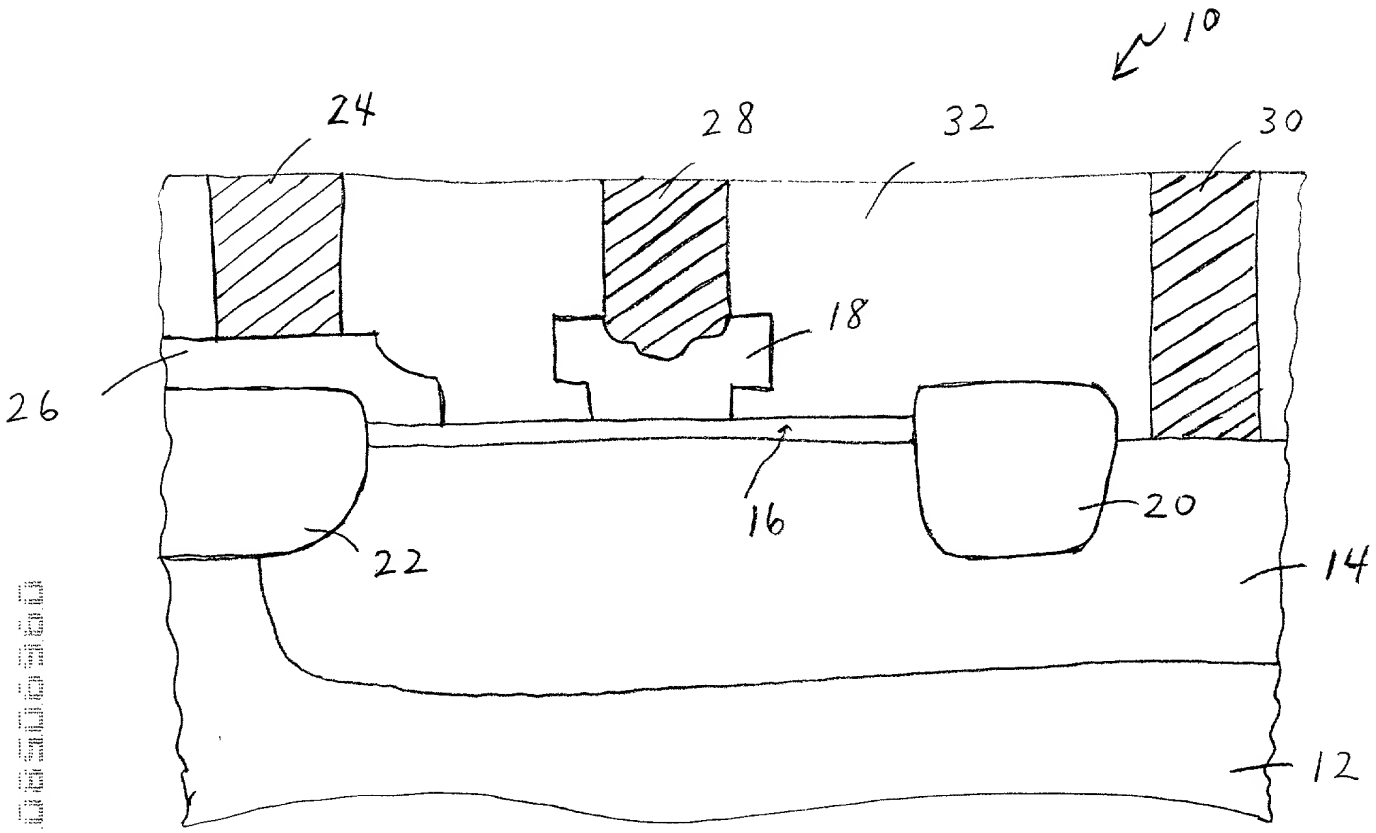

FIG. 1 PRIOR ART

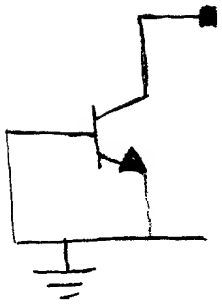

FIG. 2A
PRIOR ART

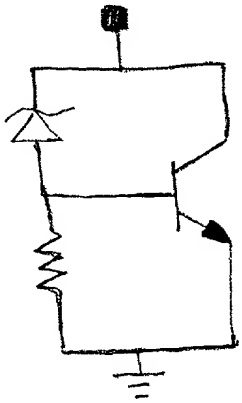

FIG. 2B
PRIOR ART

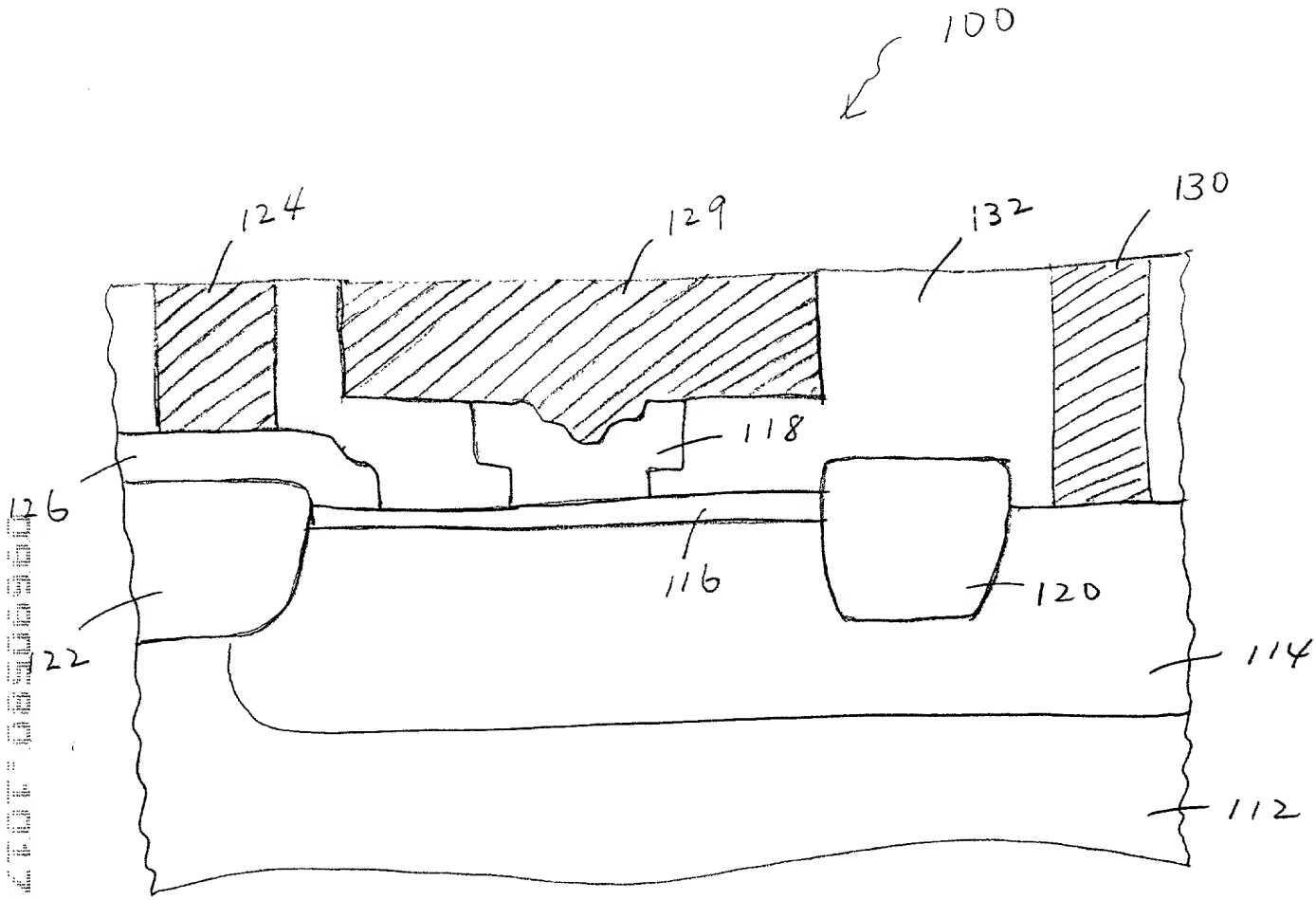

FIG 3

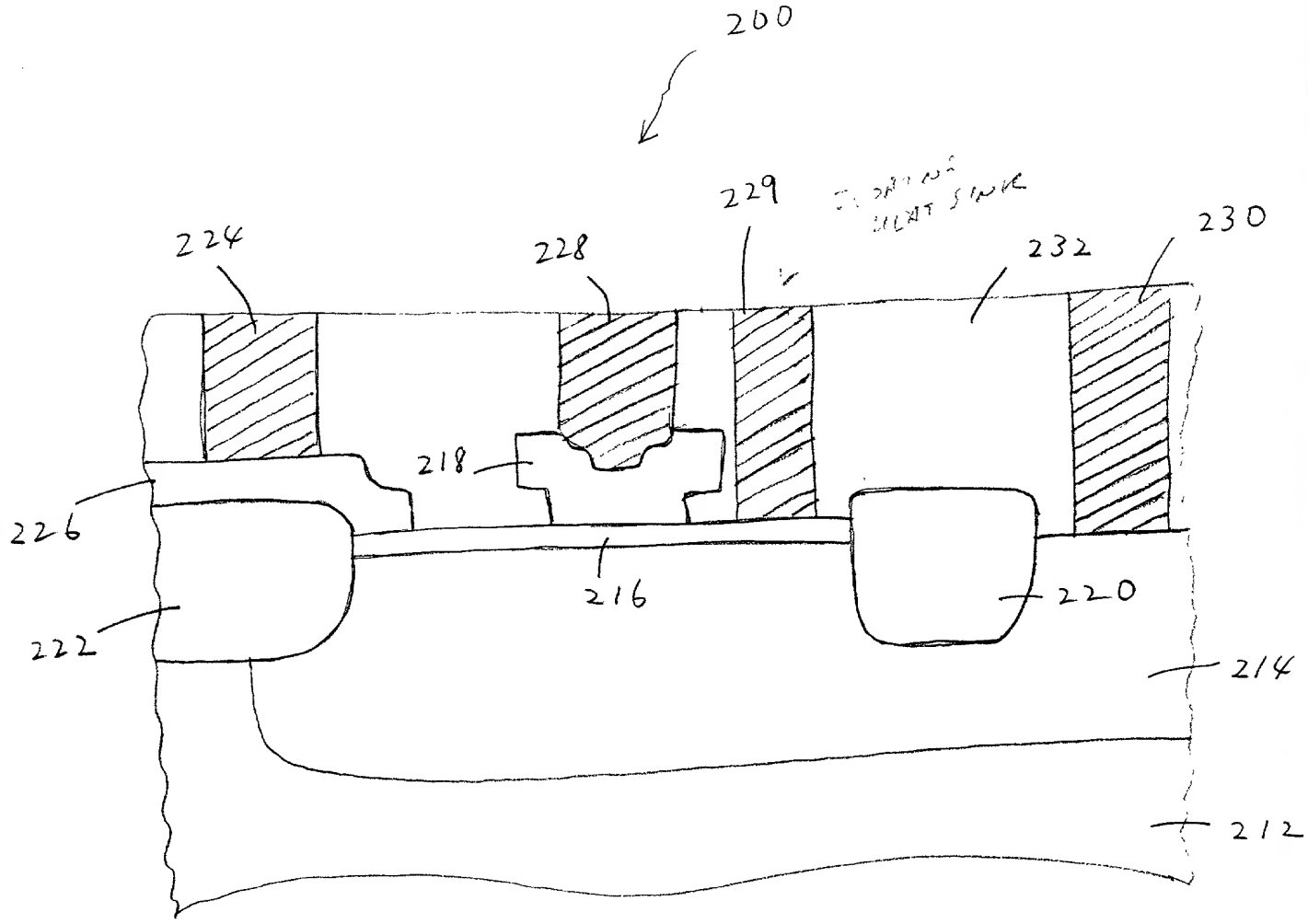

FIG. 4

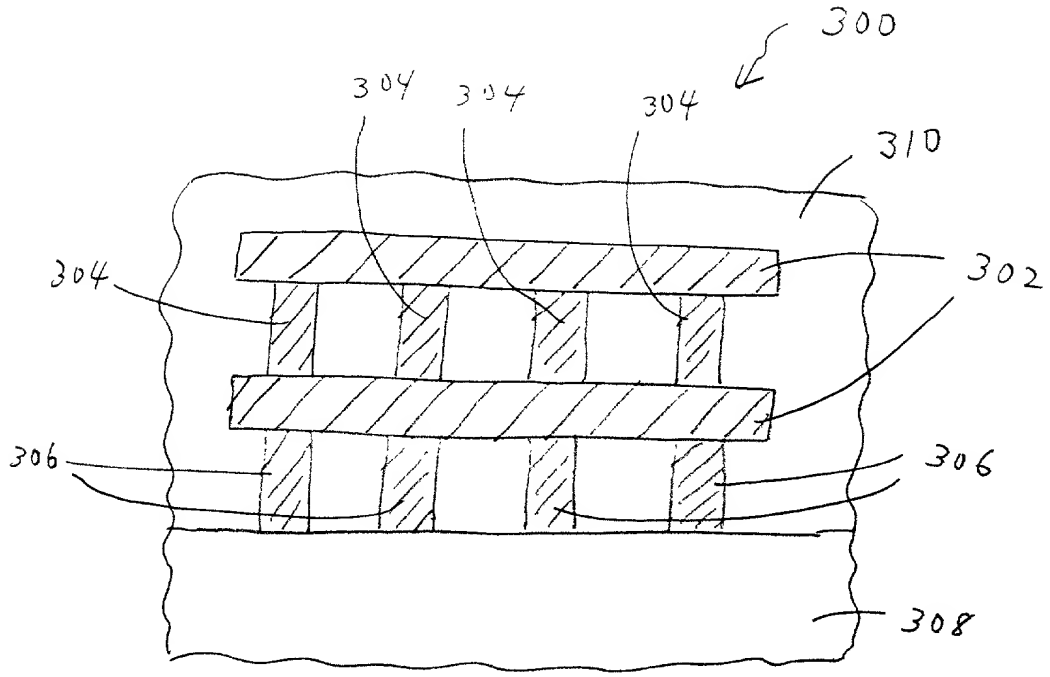
300
304
304
304
310
304
302
306
306
308

FIG 5

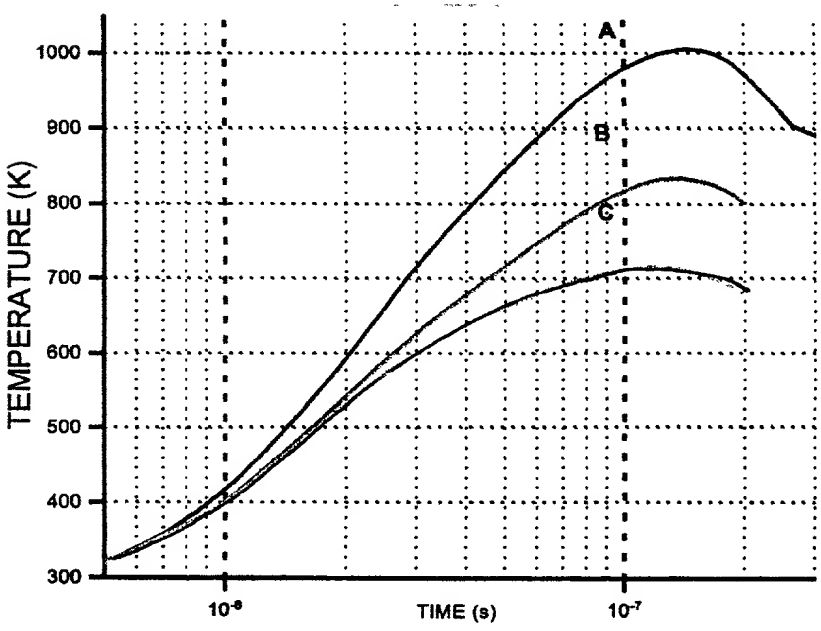
A
B
C
1000
900
800
700
600
500
400
300
TEMPERATURE (K)
10⁻⁸
TIME (s)
10⁻⁷

FIG. 6

Declaration for Patent Application English Language Declaration		
	Attorney Docket No.	NSC1-H1500-(US)
	First Name Inventor	Vladislav Vashchenko
	COMPLETE IF KNOWN:	
[X] Submitted with initial filing [ ] Submitted after initial filing (surcharge required 37 CFR 1.16(e))	Application No.	
	Filing Date	
	Group Art Unit	N/A
	Examiner	Not Yet Assigned

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

BIPOLAR TRANSISTOR-BASED ELECTROSTATIC DISCHARGE (ESD) PROTECTION STRUCTURE WITH A HEAT SINK

the specification of which (check one)

[X] is attached hereto.

[ ] was filed on _____
as United States Application No. or PCT International Application No. _____
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119 (a)-(d) or 365(b) of any foreign applications(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

			Priority Not Claimed	Certified Copy Attached	
				YES	NO
_____ (Number)	_____ (Country)	_____ (Filing Date)	[ ]	[ ]	[ ]
_____ (Number)	_____ (Country)	_____ (Filing Date)	[ ]	[ ]	[ ]
_____ (Number)	_____ (Country)	_____ (Filing Date)	[ ]	[ ]	[ ]

[ ] Additional prior foreign applications are listed on a supplemental data sheet attached hereto.

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)

☐ Additional U.S. provisional applications are listed on a supplemental data sheet attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) / Patent No. (if applicable):

☐ Additional U.S. or PCT international application numbers are listed on a supplemental data sheet attached hereto.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Vladislav Vashchenko	
Sole or first inventor's signature	Date 10.13.00
Residence Fremont, California	
Citizenship Russian Federation	
Post Office Address 39939 Stevenson Cmn. Fremont, California 94538	

Full name of second inventor Peter J. Hopper	
Second inventor's signature	Date 10.13.00
Residence San Jose, California	
Citizenship United Kingdom	
Post Office Address 4327 Verdigris Circle San Jose, California 95134	